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328612(28)

B. E. (Sixth Semester) Examination, April-May 2021

(Old Scheme)

(Et&T Engg. Branch)

ADVANCED ELECTRONIC CIRCUITS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) is compulsory from each question. Attempt any* ***two*** *parts from (b), (c) and (d).*

Unit-I

1. (a) What is the advantage of inverted R – 2R DAC over R – 2R DAC ladder network? 2

(b) Draw and explain the circuit of dual slope Analog to Digital converter in detail. 7

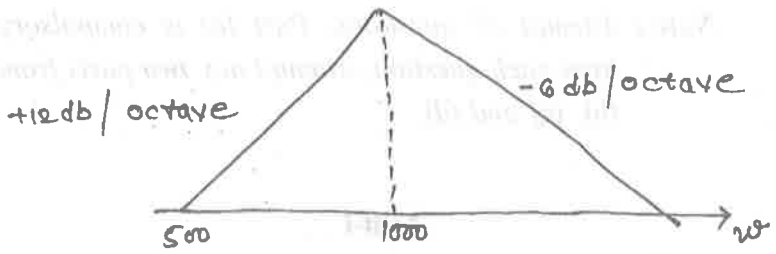
(c) Draw & explain the diagram of Delta Modulation type Analog to Digital converter. 7

(d) A 10 bit Digital to Analog converter has a step size of 10 mV. Determine the full scale output voltage and its percentage resolution. 7

Unit-II

2. (a) Explain the meaning of bilinear Transfer function. 2

(b) Design a filter for the plot given below and determine half power frequency. 7



(c) Write down different steps for designing of inverting opamp and non inverting op-amp. How can we analyse the necessity of the filter? 7

(d) What is the need to add fourth opamp in biquad circuit & also derive the expression of four opamp biquad circuit with frequency response. 7

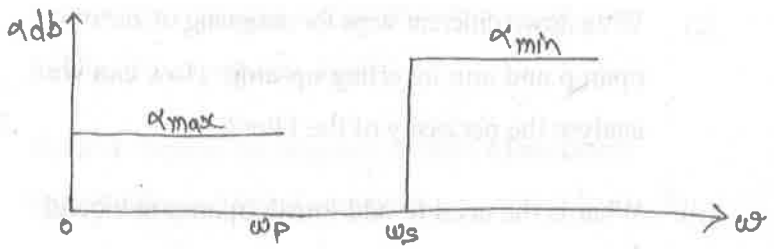
Unit-III

3. (a) Explain RC – CR transformation. 2

(b) Design a low pass Butterworth Response from the given specifications $\alpha_{max} = 0 \cdot 5$ db, $\alpha_{min} = 30$ db, $K = A_0 = 1$, $w_p = 750$ rad/sec, $w_s = 1750$ rad/sec, use scaling in the final design. 7

(c) Explain with circuit diagram the working of Deylliannis-Friend's circuit. 7

(d) The following specifications are given for a Chebyshev low pass filter : $w_p = 1$ rad/sec, $w_s = 2 \cdot 33$ rad/sec, $\alpha_{max} = 0 \cdot 5$ db and $\alpha_{min} = 22$ db design a filter. 7



Unit-IV

4. (a) Define Lock Range and Capture Range. 2

(b) A PLL has a VCO with $K_0 = 25$ kHz/V and $f_c = 50$ kHz. The amplifier gain is $A = 2$ and the phase detector has a maximum output voltage swing of ±0·7 V. Find the lock range of PLL. Assume filter gain to unity. 7

(c) Explain the operation of IC 565 VCO and explain its operation. 7

(d) Derive the expression for lock range & capture range of phase locked loop. 7

Unit-V

5. (a) What is the mean of Quadrant of multiplier? 2

(b) Draw & explain the working of logrithmic multiplier. 7

(c) Write the application of multiplier circuit & explain multiplier as phase detector. 7

(d) Explain how to get square root and square of the given analog signal? 7

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328613(28)

B. E. (Sixth Semester) Examination April-May 2021

(Old Scheme)

(AEI, EEE, EI & ET & T Engg. Branch)

ADVANCE MICROPROCESSOR & INTERFACING

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory and carries 2 marks. Attempt any* ***two*** *parts from (b), (c) and (d) of each question which carry 7 marks each.*

Unit-I

1. (a) What is the functions of different types of REP prefix?

   (b) Explain the following PIN functions of 8086 in detail?

(i) QS0 & QSI

(ii) RQ/GT0,RQ/GT1 (active low)

(iii) Lock & Test (active low)

(iv) S0, S1, S2

(c) Explain the 8086 microprocessor architecture with its register organisation in detail?

(d) The contents of different registers are given below. Form physical addresses for different addressing modes. Offset & 16 bit displacement = 5000h, AX = 1000H, DS = 2000H, BX = 1000H, SI = 3000H.

Unit-II

2. (a) What is the main difference between 8086 and 8088 microprocessor.

(b) Explain the maximum mode configuration of 8086 microprocessor in detail?

(c) Explain the different types of interrupt in 8086 microprocessor with suitable diagram of interrupt vector table.

(d) Explain the difference between minimum and maximum mode configuration.

Unit-III

3. (a) What is the main different between 8259 and 8259 A?

(b) Explain the following operating modes of IPC 8259 A.

(i) Fully Nested Mode

(ii) Automatic Rotation Mode

(iii) Buffered Mode

(iv) Cascade Mode

(c) Explain interfacing of 8254 (Programmable Interval Timer) with 8086 microprocessor with suitable diagram?

(d) Explain interfacing of DAC 0800 with 8086 microprocessor with suitable diagram.

Unit-IV

4. (a) Define the format of selector.

(b) Explain the use of each of the following register of 80386 in detail.

(i) Control Register

(ii) System Address Register

(iii) Debug & Test Register

(c) Explain the function of real mode, protected mode and virtual mode of 80386 mp in detail.

(d) Explain architecture of 80386 microprocessor in detail.

Unit-V

5. (a) Explain the multiprocessor in brief.

(b) Explain the architecture of Numeric data processor 8087 in detail.

(c) Explain the architecture of IOP (input output processor) 8089 in detail.

(d) Explain the interfacing between IOP 8089 and 8086 microprocessor with suitable diagram.

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328651(28)

B. E. (Sixth Semester) Examination April-May 2021

(New Scheme)

(Et & T Engg. Br.)

DIGITAL SIGNAL PROCESSING

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d) of each question.*

Unit - I

1. (a) Define convolution. 2

   (b) Compute circular periodic convolution of the two

sequences $x_1(n)=\{1,1,2,2\}$ and $x_2(n)=\{1,2,3,4\}$. 7

(c) Given $x(n)=\{1,2,3,4,4,3,2,1\}$, find $X(k)$ using DITFFT algorithm. 7

(d) Given : 7

$$X(k)=\{36,-4+j9\cdot656,-4+j4,-4$$
$$+j1\cdot656,-4,-4-j1\cdot656,-4j4,-4-j9.656\}$$

find $x(n)$.

Unit-II

2. (a) Define canonic and Non-canonic structures. 2

(b) Determine the direct form I realisation for a third order IIR transfer function. 7

$$H(z)=\frac{0\cdot28z^2+0\cdot319z+0\cdot04}{0\cdot5z^3+0\cdot3z^2+0\cdot17z-0\cdot2}$$

(c) Obtain a cascade realisation of the system characterised by the transfer function

$$H(z)=\frac{2(z+2)}{z(z-0\cdot1)(z+0\cdot5)(z+0\cdot4)}$$ 7

(d) Determine the parallel realisation of the IIR digital filter transfer functions.

$$H(z)=\frac{3(2z^2+5z+4)}{(2z+1)(z+2)}$$ 7

Unit-III

3. (a) List advantages of FIR filter over IIR filter. 2

(b) A low-pass filter is to designed with the following desired frequency response. 7

$$H_d(e^{jw})=\begin{cases}e^{-j2w}, & -\pi/4\le w\le\pi/4\\ 0, & \pi/4<|w|\le\pi\end{cases}$$

Determine the filter coefficients $h_d(n)$, if the window function is defined as

$$w(n)=\begin{cases}1 & , \quad 0\le n\le4\\ 0 & , \quad \text{otherwise}\end{cases}$$

determine filter coefficients of the designed filter $h(n)$.

(c) The desired response of a low pass filter is :

$$H_d\left(e^{jw}\right)=\begin{cases} e^{-j3w}, & -3\pi/4 \le w \le 3\pi/4 \\ 0, & 3\pi/4 < |w| \le \pi \end{cases}$$

Determine $H\left(e^{jw}\right)$ for $M = 7$ using a Hamming window. 7

(d) Describe the filter design procedure using Kaiser window function. 7

Unit-IV

4. (a) Define frequency warping. 2

(b) Convert the analog filter into a digital filter whose system function is :

$$H(s) = \frac{s + 0{\cdot}2}{(s + 0{\cdot}2)^2 + 9}$$

Use the impulse invariant technique.

Assume $T = 1$s. 7

(c) Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation.

Assume $T = 1$s

$$0{\cdot}9 \le \left|H\left(e^{jw}\right)\right| \le 1 \qquad 0 \le w \le \pi/2$$
$$\left|H\left(e^{jw}\right)\right| \le 0{\cdot}2 \qquad 3\pi/4 \le w \le \pi$$ 7

(d) Design a digital Chebyshev filter to satisfy the constraints

$$0{\cdot}707 \le \left|H\left(e^{jw}\right)\right| \le 1 \quad 0 \le w \le 0{\cdot}2\pi$$
$$\left|H\left(e^{jw}\right)\right| \le 0{\cdot}1 \quad 0{\cdot}5\pi \le w \le \pi$$

Using bilinear transformation and assuming $T = 1$s 7

Unit - V

5. (a) Define upsampler and downsampler. 2

(b) Obtain the expression for the output $y(n)$ in terms of $x(n)$ for the multirate systems given as follows :

$x(n) \rightarrow \boxed{\uparrow 5} \rightarrow \boxed{\downarrow 20} \rightarrow \boxed{\uparrow 4} \rightarrow y(n)$ 7

(c) Obtain the polyphase decomposition of the IIR system with transfer function :

$$H(z)=\frac{1-4z^{-1}}{1+5z^{-1}}$$ 7

(d) Obtain the two-fold expanded signal $y(n)$ of the input signal $x(n)$.

$$x(n)=\begin{cases} n, & n>0 \\ 0, & \text{otherwise} \end{cases}$$ 7

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328652(28)

B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(Et & T Branch)

ELECTRONIC CIRCUIT DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) is compulsory and carries 2 marks and, attempt any two from part (b), (c) & (d) and carries 7 marks.*

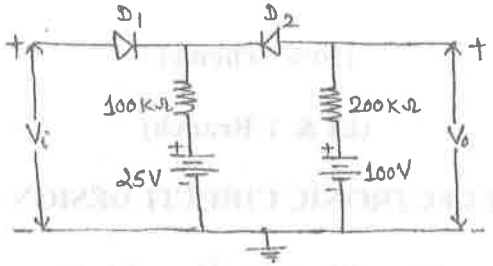
Unit - I

1. (a) Calculate oscillation frequency of the square wave generator whare $R = 10\,k\Omega$ and $C = 0{\cdot}01\ \mu F$.

   (b) Draw the circuit of Triangular wave generator using

OPAMP and explain its operation.

(c) The input voltage V_i to the two level clipper shown in figure varies linearly from 0 to 150 volt. Sketch the output voltage V_o to the same time scale as the input voltage. Assume ideal diodes.



(d) Draw and explain current sweep generator in details.

Unit - II

2. (a) What is a multivibrator? Give the names of different types of multivibrator.

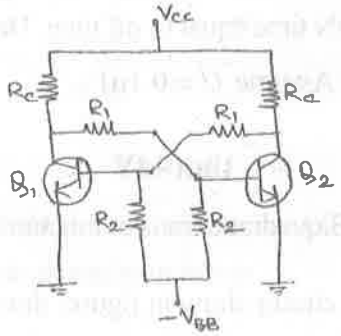
(b) With the help of a schematic diagram explain how the commutating capacitor reduces the transition time.

(c) The fixed-bias binary shown in figure uses n-p-n

silicon transistor with $V_{CE(sat)} = 0{\cdot}5V$, $V_{BE(sat)} = 1V$, $I_{CBO} = 10nA$ at 25°C and zero base to emitter voltage at cut-off. The circuit parameters are $V_{CC} = V_{BB} = 6V$, $R_C = 1{\cdot}2k\Omega$, $R_1 = 4{\cdot}7k\Omega$, $R_2 = 27k\Omega$. Find :

(i) h_{FE}(min) and stable state voltages and currents.

(ii) If the reverse saturation current doubles for every 10°C rise in temperature, what is the maximum temperature at which the circuit can operate properly with one device remaining off?



(d) Draw and explain schmitt trigger circuit. Write

some applications of this circuit.

Unit - III

3. (a) Why normally control terminal of IC-255 timer is connected to ground through 0·01 μF by pass capacitor?

(b) With neat circuit diagram explain astable multivibrator using IC-555. Also derive the relation for its duty cycle.

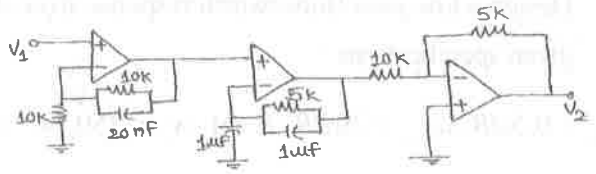
(c) Discuss how monoshot can be used as missing pulse detector?

(d) Design an astable multivibrator which will flash an electric bulb such that its on time will be 3 second and off time will be 1 second. Modify the circuit to get ON time equal to off time. Design both the circuits. Assume $C = 0{\cdot}1\mu F$.

Unit - IV

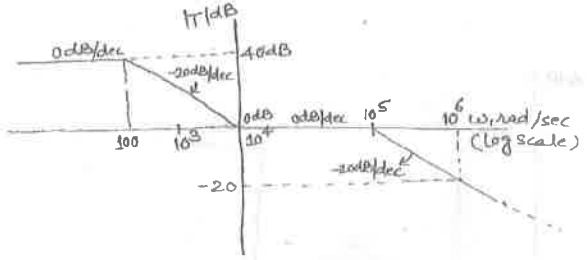
4. (a) Define Biquadratic transfer function.

(b) For the circuit show in figure, draw asymptotic Bode plot for magnitude $T(3w)$.



(c) Explain Biquad circuit with circuit diagram and also derive an expression for frequency response.

(d) The accompanying figure shows the asymptotic Bode plot for a desired magnitude response. Design an amplifier filter using a minimum number of OPAMP. Give the schematic and indicate the element values for your design.



Unit - V

5. (a) Differentiate Butterworth filter and Chebyshev filter relative to attenuation factor.

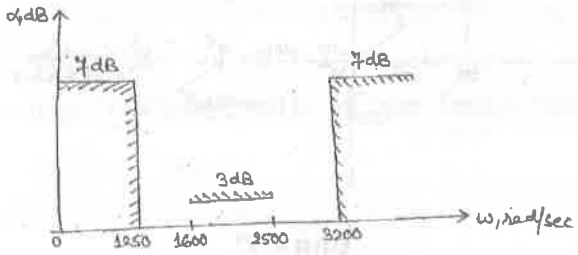
(b) Define sensitivity. Explain the sensitivity analysis of sallen and key circuit.

(c) Design a low pass Butterworth response from the given specifications :

$\alpha_{max} = 0.5\,dB,\ \alpha_{min} = 30\,dB,\ K = 1,\ w_p = 750,\ w_s = 1750$

use scaling in final design.

(d) Design a bandpass filter to meet the specification shown in figure with the added requirement that the response be Butterworth. It is required that $\alpha(2000) = 0$. Show steps in the Geffe algorithm carefully. In your final design, at least one capacitor should have the value of 0·1 μF.



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328653(28)

B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(Et & T Branch)

MICROCONTROLLER & EMBEDDED SYSTEMS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *All questions are compulsory and carry equal marks. Part (a) is compulsory, attempt any two parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) What do you understand from OTP microcontroller? What are the advantages using OTP microcontrollers? 2

(b) Write a table of features of MCS51 family for any six microcontrollers manufactured by DALLAS semiconductors. Which microcontrollers among these have NVRAM and UVRAM program memory? 7

(c) Draw a basic practical Application circuit using 8051 showing clocking circuit, power on reset circuit and pull up register network for port 0. Why pull up registers are necessry for port 0 only and not for other ports of 8051? Explain using proper port structure for port 0? 7

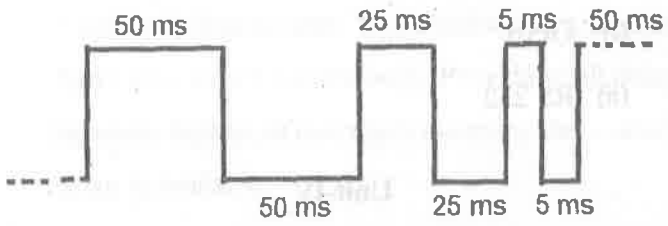
(d) Draw the RAM structure for 8051. In 8052, address space 80 H to FFH is used for SFR's as well as RAM then, how both of them will be accessed using same addresses? Explain with examples of instructions used for accessing RAM location and SFR assigned with same address. 7

Unit-II

2. (a) Define Interrupts and Polling in very brief. 2

(b) In certain industry a fire alarm system is implemented which produces high to low transition pulse at output whenever the smoke sensor detect smoke due to fire. If this high to low transition pulse is applied at port pin P 3·2 (INT 0) of 8051, write software to sound an alarm and flash indicator lamp continuously unit reset of the fire system. 7

(c) If a crystal frequency for 8051 microcontroller is 16 MHz, generate 100 cycles of following waveform at port pin P 2·0. 7



(d) Write a note on MODE 3 (split timer mode) of timer in 8051. 7

Unit-III

3. (a) What is data framing? Show Framing of character "B" between one start and one stop pulse. 2

(b) Write a program to transfer a string of data "Wish you a very happy Birthday". Serially at the baud rate 9600. XTAL is 11·0592 MHz and data string is to be taken from code memory from an address 0400 H. 7

(c) Write a program to receive a data string "Thank you very much". Serially at the baud rate 9600. XTAL is 11·0592 MHz. Save the received data string at an address 1000H of external memory. 7

(d) Write a note on any **one** bus standard : 7

(i) GPIB

(ii) RS 232

Unit-IV

4. (a) Write a function of $\overline{EA}$/Vpp and $\overline{PSEN}$ pin in memroy interfacing. 2

(b) For a certain application it is required to have 256 KB of NVRAM data memory in a 8051 memory system. Draw the memory interfacing hardware and show how 256 KB memory is accesses using 64 KB blocks. 7

(c) A Port pin P 1·1 is connected to a switch SW. Assuming that a stepper motor connected to P 2·0 – P 2·3 has step angle 2°, write a program to do following :

(i) If SW = 0, Move stepper motor clockwise for one complete revolution.

(ii) If SW = 1, Move stepper motor anticlockwise for one complete revolution. 7

(d) Draw hardware circuit diagram for a 7 segment display system using 8051 and one common cathode 7 segment display unit. Write software to display digits from 0 to 9 continuously. Provide small delay between displays of two digits assuming that a small delay is available. 7

Unit-V

5. (a) Define real time embedded system. 2

(b) Design an embedded system (block diagram only) for any real life application. Explain its functioning in detail. 7

(c) Write all the characteristics of a real time embedded system. 7

(d) What are different design phase challenges and issues during development of an embedded system? 7

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328654(28)

B. E. (Sixth Semester) Examination April-May 2021

(New Scheme)

(Et&T Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory, which is of 2 marks. Attempt any* **two** *parts from (b), (c) and (d) each is of 7 marks. Assume suitable data wherever necessary. Draw the diagram to support your answer if required.*

Unit-I

1. (a) What is Moore's law? 2

(b) Consider an n-channel MOS system that is characterized by x_{ox} = 100 Å and Na = $10^{15}/cm^3$. An n-type poly gate is used with $N_{d, poly} = 10^{19}/cm^3$. The fixed oxide charge is approximated as $Q_f = q\,(10^{11})$ c/cm^2 and is the dominant oxide charge term, and the acceptor ion implant dose is assumed to be $D_I \approx 2\times10^{12}$ /cm^2. Determine the threshold voltage. 7

(c) Explain the term switching intervals and derive an expression for fall time (t_f) in CMOS inverters. 7

(d) Draw the complete VLSI Design flow for programmable logic devices and Application Specific Integrated Circuits (ASIC). 7

Unit-II

2. (a) Write the significance of Euler graph to draw stick diagram or layout for any complex logic circuit. 2

(b) Describe photolithography process for VLSI circuits and role of positive & negative photoresist to draw various patterns. 7

(c) Explain the basic sequence of processes to fabricate *n*-well CMOS inverter. 7

(d) Write the MOSIS Lamda (λ) based layout design rules for active area, polysilicon, metal and contacts. 7

Unit-III

3. (a) Write the difference between stick diagram & layout representation of the circuit. 2

(b) Draw the pass transistor based circuit diagram & layout for 4 : 1 multiplexer. 7

(c) Draw the circuit diagram for 6 T SRAM & explain the read and write operations. 7

(d) Draw the CMOS layout of J-K flip-flop. 7

Unit-IV

4. (a) Write the critical difference between Concurrent & Sequential Assignment Statements. 2

(b) Consider the function $f(x_1, x_2, x_3) = \sum m$

$(2, 3, 4, 6, 7)$. Show how it can be realized using 2, two input LUT's only. 7

(c) With the use of Generate syntax, write the VHDL code to design 16 : 1 multiplexer using 4 : 1 multiplexer as a component. 7

(d) Explain process statements of VHDL, including general syntax of process, sensitivity list, process declarative items, sequential statements and example. 7

Unit-V

5. (a) Define the term test vectors in test bench source code. 2

(b) Write a VHDL code of Moore type FSM (Finite State Machine) for serial adder. 7

(c) Write a VHDL code to design Mealy FSM (Finite State Machine) to detect a bit sequence 101. 7

(d) Write a VHDL code which describes a simple test bench for half adder. 7

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328655(28)

B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(ET&T Engg. Branch)

INFORMATION THEORY & CODING

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory and carries 2 marks. Attempt any two parts from (b), (c) and (d) of each question and carries 7 marks.*

Unit-I

1. (a) Write the difference between lossless and lossy compression.

(b) An analog signal having 4 kHz bandwidth is sampled at 1.25 times the Nyquist rate and each sample is quantized into one of 256 equally likely levels. Assuming that the successive samples are statistically independent.

(i) What is the information rate of this source?

(ii) Can the output of this source be transmitted without error over an AWGN channel with a bandwidth of 10 kHz and S/N ratio of 20 dB?

(iii) Find the S/N ratio required for error-free transmission for part II?

(iv) Find the BW required for an AWGN channel for error free transmission of the output of this source if the S/N ratio is 20 dB.

(c) Write Lempel Ziv-Algorithm.

(d) A binary channel is having following noise characteristics :

$$\begin{bmatrix} 2/3 & 1/3 \\ 1/3 & 2/3 \end{bmatrix}$$

(i) If the input symbol are transmitted with probability 3/4 and 1/4 respt. Calculate $H(X)$, $H(Y)$, $H(X, Y)$, $H(X/Y)$ and $H(Y/X)$.

(ii) Find channel capacity, efficiency and redundancy.

Unit-II

2. (a) Define syndrome, error detection and correction capacity.

(b) Consider a (7, 4) block code with generator matrix

$$G = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

Determine whether the following received words are valid codeword

(i) 0001101

(ii) 0110101

(c) Generate a (7, 4) systematic cyclic code. Write all codes using generated matrix. Design decoding method using parity check matrix. If following code words are received, find corrected code words.

(i) 1101101

(ii) 0101000

(d) The generator polynomial for (7, 4) cyclic Hamming code is given as $G(x) = 1 + x^1 + x^3$ generated code polynomials in non systematic form for message vector $m_1 = 1010$, $m_2 = 1001$.

Unit-III

3. (a) Define primitive element and minimal polynomial.

(b) Construct the extension field GF (16) by assuming the primitive polynomial $P(y) = y^4 + y + 1$ over GF (2). Also assume the $\alpha = y$, obtain the elements of GF (16) and minimal polynomial as well.

(c) Explain decoding procedure for a single bit and multiple bit error correction BCH code.

(d) Construct the extension field GF (16) from G (4) assuming the primitive polynomial $P(y) = y^2 + y + 1$. Also obtain all the minimal polynomial.

Unit-IV

4. (a) Define code rate of convolution code.

(b) Consider convolution encoder given below has the following two generator sequences each of length 3.

$\left(g_0^{(1)}, g_1^{(1)}, g_2^{(1)}\right) = (1, 1, 1)$ and $\left(g_0^{(2)}, g_1^{(2)}, g_2^{(2)}\right) = (1, 0, 1)$

Obtain the encoder sequence for the input message.

$(m_0, m_1, m_2, m_3, m_4) = (1, 0, 0, 1, 1)$

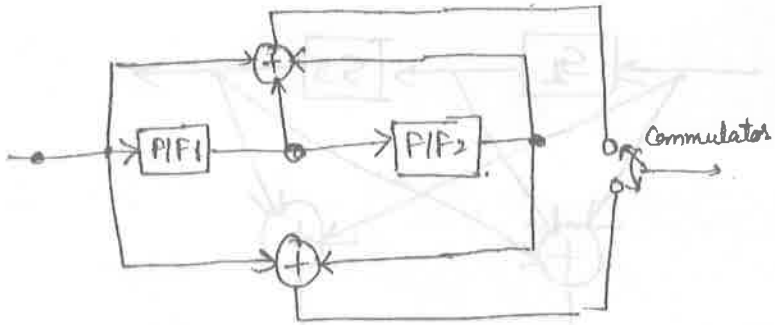


Fig : Convolution encoder

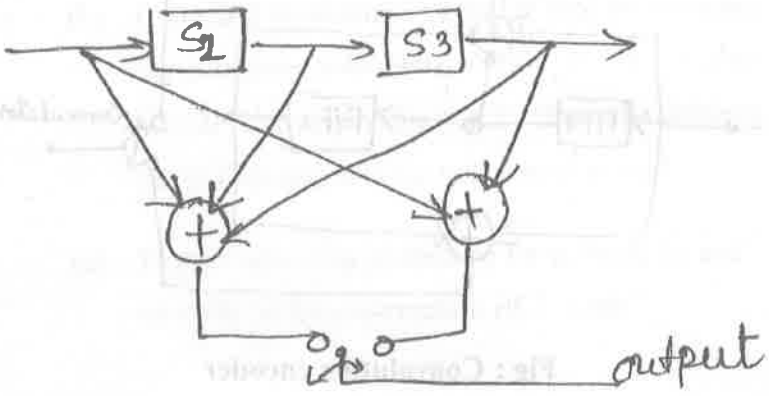
(c) Generator vectors for a rate 1/3 convolution encoder are $g_1 = (1, 0, 0)$; $g_2 = (1, 0, 1)$; $g_3 = (1, 1, 1)$

(i) Draw encoder diagram

(ii) Draw trellis diagram

(iii) Using trellis find code vector if message vector is (101100).

(d) For the encoder shown generates an all zero sequence which is sent over binary systematic channel. The received sequence 01001000.... There are two error in this sequence (2^{nd} and 5^{th}) show that this double error detection is possible with correction by application of Viterbi algorithm.



Unit-V

5. (a) Define free Eucledean Distance.

(b) Explain in details Ungerbock's TCM Design Rules, also explain TMC decoder.

(c) Explain with the help of one example how a trellis encoder can be combined with a modulator to give Trellis coded modulation.

(d) Explain the procedure of mapping by set partitioning. Why this process is done?

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B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(Et & T Branch)

INTERNET & WEB TECHNOLOGY

(Professional Elective-I)

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

***Note** : Part (a) of each unit is compulsory and carries 2 marks. Attempt any two parts from (b), (c) and (d) which carry 7 marks each.*

Unit-I

1. (a) Define Internet. 2

   (b) Explain HTTP and HTTPS in detail. 7

(c) Explain difference between TCP and UDP. 7

(d) Short notes on JSP, ASP and JZEE. 7

Unit-II

2. (a) What is HTML? 2

(b) Describe HTML, It's feature, HTML elements and attributes. 7

(c) What is CSS? What are the advantages of using CSS. 7

(d) What is Java Script? Describe difference between Java and Java Script. 7

Unit-III

3. (a) What is XML? 2

(b) Describe DTD, its types and syntax. 7

(c) Describe XML schema in detail. 7

(d) Explain XML name space with example. 7

Unit-IV

4. (a) What is Virus? 2

(b) Describe various electronic payment system in detail. 7

(c) Describe Firewall and it's types. 7

(d) Describe EDI system and it's benefits. 7

Unit-V

5. (a) Define the term Website. 2

(b) Describe Web Hosting and webserver. What are the services given by web hosting companies. 7

(c) Describe FTP (File Transfer Protocol) in detail. 7

(d) Short notes on Telnet and search engine. 7

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B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(Et&T Engg. Branch)

OPERATING SYSTEM

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

***Note** : Part (a) is compulsory in each unit. Attempt any **two** parts from (b), (c) and (d).*

Unit-I

1. (a) What are the advantages of multiprocessing systems? 2

(b) What is an Operating System? What are the services offered by it? 7

(c) Describe in brief what are the file allocation and access methods? 7

(d) Write short notes on : 7

(i) Acyclic Graph Directories

(ii) File Protection

Unit-II

2. (a) Define the contents of Process Control Block. 2

(b) Explain any three CPU scheduling algorithms and their evaluation. 7

(c) Suppose a disk drive has 5000 cylinders, numbered 0 to 4999. The drive is currently serving a request at cylinder 143 and the previous was at cylinder 125. The queue of pending requests in FIFO order is

86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130

What is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for SSTF, SCAN and C-LOOK. 7

(d) Consider the following set of processes, with the length of the CPU-burst time give in milli seconds.

Process	Burst Time	Priority
P_1	10	3
P_2	1	1
P_3	2	3
P_4	1	4
P_5	5	2

The process are assumed to have arrived in the order P_1, P_2, P_3, P_4, P_5 all at time 0.

(i) What is the turn around times for FCFS, SJF, priority (smaller priority no. implies higher priority) and RR (quantum = 1) scheduling.

(ii) What is the waiting time for the above scheduling algorithms?

(iii) Which of the algorithm results in minimal average waiting time? 7

Unit-III

3. (a) Explain memory protection in brief. 2

(b) How is performance of demand paging measured? Explain how degree of multiprogramming is related to thrashing? 7

(c) What is Paging? How is it different from segmentation? 7

(d) Explain the following with the help of an example : 7

(i) First Fit

(ii) Best Fit

(iii) Worst Fit

Unit-IV

4. (a) What are the necessary conditions for deadlock? 2

(b) Explain the importance of semaphores in concurrency? How are they implemented? 7

(c) What is meant by deadlock avoidance and deadlock prevention? Explain safety algorithm. 7

(d) Explain Readers Writers classical problem of concurrency. Write the code for it. 7

Unit-V

5. (a) Discuss the structure of Unix O.S. 2

(b) Discuss the layered architecture of I/O software. Explain the importance of each layer. 7

(c) What are distributed file systems and what is meant by location independence and two level naming? 7

(d) What are the various performance evaluation techniques? Explain them in brief. 7

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B. E. (Sixth Semester) Examination, April-May 2021

(New Scheme)

(Et&T Branch)

COMPUTER ORGANIZATION & ARCHITECTURE

(Professional Elective-I)

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Part (a) of the entire question is compulsory. Part (a) carries 2 marks. Attempt any two parts from part (b), (c) and (d). Part (b), (c) and (d) carries 7 marks.*

Unit-I

1. (a) Draw the basic functional units of a computer. 2

   (b) Explain memory locations and addressess. 7

(c) Discuss about different types of addressing modes. 7

(d) Explain in detail about different instruction types and instruction sequencing. 7

Unit-II

2. (a) What is control store? 2

(b) Draw and explain typical hardware control unit. 7

(c) Write short notes on :

(i) Micro instruction format

(ii) Symbolic micro instruction 7

(d) Draw and explain about micro program control unit. 7

Unit-III

3. (a) Draw a diagram to implement manual multiplication algorithm. 2

(b) Explain in detail about different instruction types and instruction sequencing. 7

(c) How floating point addition is imlemented? Explain briefly with a neat diagram. 7

(d) Write an algorithm for the division of floating point number and illustrate with an example. 7

Unit-IV

4. (a) List out the types of interrupts. 2

(b) Explain with the block diagram the DMA transfer in a computer system. 7

(c) Discuss the design of a typical input or output interface. 7

(d) Explain the action carried out by the processor after occurrence of an interrupt. 7

Unit-V

5. (a) What is memory interleaving? 2

(b) Illustrate the characteristics of some common memory technologies. 7

(c) Describe in detail about associative memory. 7

(d) What do you mean by virtual memory? Discuss how paging helps in implementing virtual memory? 7