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B028312(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2020

(New Scheme)

(Electronics and Telecommunication Engg. Branch)

ELECTRONICS DEVICES

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) is compulsory. Attempt any two parts from (b), (c) and (d). Draw neat, labeled diagrams wherever necessary.*

Unit-I

1. (a) (i) Define mobility and conductivity. 2

(ii) What is difference between diffusion and drift currents? 2

(b) Define a graded semiconductor. Explain why an electric field must exist in a graded semiconductor? Derive the expression for potential variation in graded semiconductor. 8

(c) (i) State Mass-Action law as an equation and in words 2

(ii) Discuss the potential variation, electric field and charge density inside depletion layer of p-n junction. 6

(d) (i) Determine the concentration of free electronics and holes in a sample of germanium at 300°K which has a concentration of Donor atoms equal to 2×10^{14} atoms/cm^3 and concentration of acceptor atoms equal to 3×10^{14} atoms/cm^3. Is this a p-type or n-type Ge. In other words is the conductivity due primarily to holes or to electronics. 5

(ii) Repeat part (i) for equal donor and acceptor concentration of 10^{15} atoms/cm^3. Is this p-type or n-type Ge? 3

Unit-II

2. (a) (i) Draw V-I characteristics of ideal and practical p-n junction silicon diode. 2

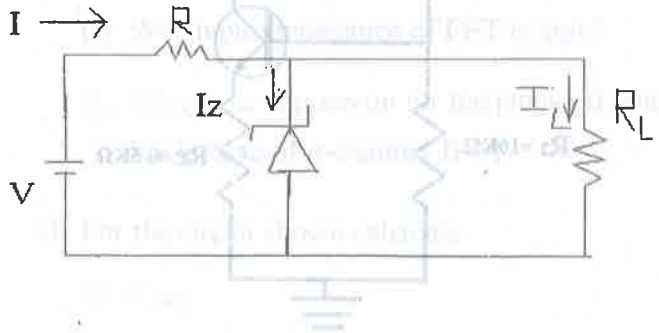
(ii) Define peak inverse voltage. 2

(b) Draw the circuit diagram of full-wave bridge rectifier and derive the efficiency, ripple factor, PIV, TUF. 8

(c) Explain zener diode as voltage regulator. Derive equations for variable source and load. 8

(d) (i) The Avalanche diode shown regulates at 50 V from 5 to 40 mA current. The supply voltage V is 200 V. Calculate R to allow voltage regulation from $I_L = 0$ to $I_L = I_{L\,max}$. What is $I_{L\,max}$? 4

(ii) If R is set as above but I_L is fixed at 25 mA then what is the permissible range of V. 4



Unit-III

3. (a) (i) What is a transistor? Why is it so called? 2

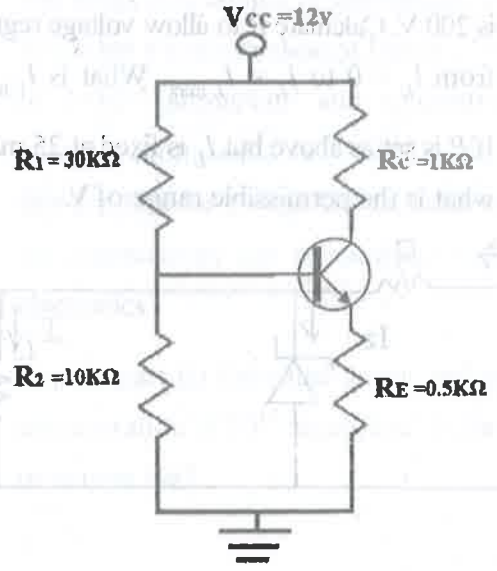
(ii) What is thermal runaway? 2

(b) Draw Eber-Moll model of a transistor for a npn transistor and explain the same. 8

(c) For the circuit shown : 8

(i) Find the operating point.

(ii) What is the stability factor of the circuit. Given $\beta = 50$, $V_{BE} = 0{\cdot}7\ v$? 8



(d) Draw the circuit for transistor in CE configuration and draw the input output characteristics of common emitter configuration. Explain in characteristics the transistor active region, saturation and cut off region giving one application each. 8

Unit-IV

4. (a) (i) FET is a voltage controlled device. Justify. 2

(ii) Define pinch off voltage. 2

(b) Explain the construction and working of a n-channel JFET with drain current equation. Also draw drain and transfer characteristics. 8

(c) (i) Explain why does the drain current ID not reduced to zero even after the channel is pinched off?

(ii) Why input impedance of FET is high?

(iii) Obtain the expression for the pinch off voltage VP in case of *n*-channel JFET. 8

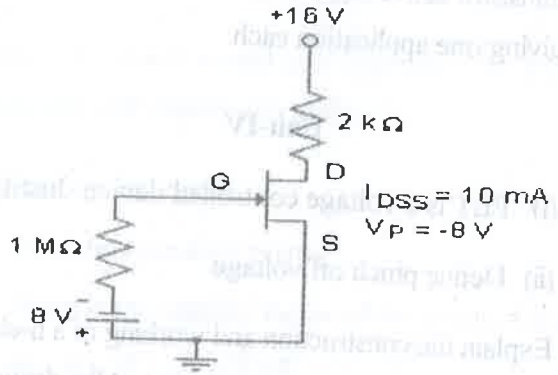
(d) For the circuit shown calculate : 8

(i) V_{GSQ}

(ii) I_{DQ}

(iii) V_{DS}

(iv) V_D



Unit-V

5. (a) (i) Draw symbol of *n*-channel E-MOSFET and *n*-channel D-MOSFET. 2

(ii) Why is MOS transistor devices are commercially more important than JFET? 2

(b) Draw and explain the typical volt ampere drain characteristics and the transfer characteristics of an *n*-channel MOSFET transistor operated both in enhancement mode and depletion mode. 8

(c) Explain the construction and working of enhancement MOSFET with neatly labeled diagrams. 8

(d) Write short notes on : 4×2=8

(i) Sub threshold conduction

(ii) MOS switch

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B.Tech. (Third Semester) Examination

Nov.-Dec. 2020

(New Scheme)

DIGITAL SYSTEM DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Attempt all questions. Part (a) is compulsory & Solve any two parts from (b), (c) and (d) of each questions.

Unit-I

1. (a) Write the Distributive Laws. 2

(b) Using Boolean Algebra, prove that : 7

(i) $AB + ABC + A\bar{B} = A$

(ii) $(B+A)(B+D)(A+C)(C+D) = BC + AD$

(iii) $AB + A'C = (A+C)(A'+B)$

(c) Reduce using mapping the following Boolean function in : 7

(i) Sum of products

(ii) Product of sums

Also implement it using Universal Gates

$F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$

(d) Reduce the following expression using tabular method. 7

$F(A, B, C, D) = \sum m(0, 2, 3, 5, 8, 10, 11, 13)$

Unit-II

2. (a) Differentiate between combinational and sequential circuits. 2

(b) Design a Full adder circuit using Decoder. 7

(c) Draw the neat & clean diagram of BCD Adder and explain its working through table. 7

(d) What is Multiplexer? Write down its application and draw 16 : 1 multiplexer using only 2 : 1 multiplexer. 7

Unit-III

3. (a) Write difference between Latch and flip-flop. 2

(b) Draw the logic diagram of J-K flip-flop and explain its working to : 7

(i) Obtain the flip-flop characteristics table

(ii) Obtain characristics equation

(iii) Obtain excitation table

(c) Design BCD Ripple Counter and explain its functioning. 7

(d) What is Shift Register? Explain various types of shift register in brief. 7

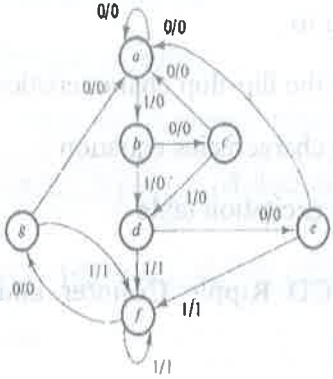
Unit-IV

4. (a) Compare Moore & Mealy FSM. 2

(b) What is Algorithmic State Machines charts? List the silent features of the ASM charts. 7

(c) Design a Pulse train generator using a shift register to generate the following waveform : 7

(d) Reduce the number of states in the following state table and tabulate the reduced state table and also draw the reduced state diagram. 7



Unit-V

5. (a) Define Fan-in and Fan-out. 2

(b) Give comparison among various logic families. 7

(c) Draw the circuit diagram and explain the operation of 2 inputs TTL NAND gate with totem - pole output. 7

(d) Draw two input CMOS NAND & NOR gate and explain their operations. 7

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B028315(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2020

(New Scheme)

DATA STRUCTURE USING C++

(ET & T Engg. Branch)

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Attempt all questions. Part (a) carries 4 marks and is compulsory. Attempt any* ***two*** *parts from part (b), (c) and (d) carrying 8 marks each.*

Unit-I

1. (a) What is default constructor and what is the advantage of having it.

(b) Write a program using the concept of array of objects.

(c) Write a program in C++ to keep 1000 records of books [ACC-No, Name, Cost] and make a function to display all records.

(d) What is a friend function? Write a program to declare friend function in two classes.

Unit-II

2. (a) Differentiate between function overloading and function overriding.

(b) Write a program using the concept of multiple inheritance.

(c) Define operator overloading? Write a program to overload '+' operator to add two complex numbers.

(d) Define inheritance? Explain different types of inheritance.

Unit-III

3. (a) Explain the concept of abstract class in brief.

(b) Define pointer. Explain memory management operator in C++.

(c) Explain this pointer. Write a program to use this pointer.

(d) What is virtual function? Write a program to declare virtual display function in base class.

Unit-IV

4. (a) Define data structure and its types.

(b) Define sorting. Explain selection or bubble sort with an example.

(c) Explain the concept of linear search. Write a program to search an element in an array of integers (linear search).

(d) Define Queue. Write a C++ program to add an element in a queue and delete an element from the queue.

Unit-V

5. (a) What are the advantages of link-list over array?

(b) Explain Binary search tree with suitable example.

(c) Explain different types of tress with example.

(d) Explain different traversing techniques for Graph.

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B033315(033)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2020

DIGITAL ELECTRONICS

Time Allowed : Three hours

Maximum Marks : ~~80~~ 100

***Note** : Attempt all questions. Each question carries equal makrs. Part (a) is compoulsory and answer any **two** from (b), (c) and (d).*

Unit-I

1. (a) Find the 9's complement of : 2 4

(i) 3465

(ii) 782·54

(b) Perform the following decimal addition in 8421 code : 7 8

679·6 + 536·8

(c) Write short notes on : 7 8

(i) XS-3 code

(ii) Cyclic code

(iii) Gray code

(iv) 8421 code

(d) Using Quine Mc-cluskey simplyfy the following : 7 8

$$F(A, B, C, D) = \Sigma m(0, 1, 3, 7, 8, 9, 11, 15)$$

Unit-II

2. (a) Define Half adder. 2 4

(b) Implement a 16 : 1 multiplexer using 4 : 1 multiplexer. 7 8

(c) Design a carry look ahead adder 7 8

(d) Design a full substractor. 7 8

Unit-III

3. (a) Define sequential circuit. 2 4

(b) Explain the working of Bi-directional shift register with logic diagram. 7 8

(c) Explain the race around condition for J-K flip flop. How can it be avoided in master-slave flip-flop? 7 8

(d) Draw and explain the working of 3 bit UP synchronous counter. 7 8

Unit-IV

4. (a) Define flip-flop. 2 4

(b) Differentiate between Moore and Mealy machines. 7 8

(c) Convert JK flip-flop to D flip-flop 7 8

(d) Convert SR flip-flop to T flip-flop 7 8

Unit-V

5. (a) Define Memory 2 4

(b) Draw and explain Nand gate totem pole TTL. 7 8

(c) Implement the following function using PLA : 7 8

$$F(A, B, C, D) = AC' + A'B'C' + ABCD$$

(d) Explain briefly ROM organization. 7 8

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B067313(067)

B.Tech. (Third Semester) Examination
Nov.-Dec. 2020

ELECTRONIC DEVICES and DIGITAL CIRCUITS

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Attempt all questions. Part (a) is compulsory & Attempt any* ***two*** *parts from (b), (c) and (d) of each questions.*

Unit-I

1. (a) What is static resistance of a diode? 4

(b) Sketch the V-I characteristics of a diode and explain it. 8

(c) Explain the working of a half wave rectifier with circuit diagram and waveforms. 8

(d) Explain Zener breakdown and differentiate it from Avalanche breakdown. 8

Unit-II

2. (a) Why is the base most lightly doped? 4

(b) Draw the circuit diagram and explain the working of a transistor in CB configuration. 8

(c) With a neat diagram explain the V-I characteristics of JFET. 8

(d) Draw and explain the construction and working of a depletion type MOSFET. 8

Unit-III

3. (a) Define universal gates. 4

(b) Simplify the following Boolean function by K-map. 8

$$F = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12)$$

(c) Explain all logic gates in brief. 8

(d) Explain the basic concept of TTL to implement universal logic gate. 8

Unit-IV

4. (a) Define Combinational circuit with basic block diagram. 4

(b) Explain FULL-ADDER using two HALF Adder with its logic diagram. 8

(c) Define Multiplexer. Explain 2-input and 4-input Multiplexer with suitable block diagram. 8

(d) Define Decoder. Explain 3 to 8 Line Decoder with Block Diagram. 8

Unit-V

5. (a) What is Shift Register? 4

(b) Draw the conversion of JK Flip to RS Flip flop using all necessary steps. 8

(c) Explain parallel in serial out shift register using block diagram. 8

(d) Design a D- Flip Flop using 8

(i) Logic Diagram

(ii) Graphical Symbol

(iii) Truth Table

(iv) Characteristics Table

(v) Excitation Table

(vi) Characteristics Equation (K-map Table)