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B024314(024)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

A) CTE (~~New~~ Scheme)

DIGITAL ELECTRONICS

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) What is Parity bit? Explain. 4

   (b) (i) Convert gray code 101011 into its binary equivalent. 2

(ii) Convert $(85{\cdot}63)_{10}$ to binary. 2

(iii) Convert $(2AC5{\cdot}D)_{16}$ to decimal. 2

(iv) Convert $(475{\cdot}25)_{8}$ to decimal. 2

(c) What is the simplified form of the Boolean expression?

(i) $ABC' + ABC + A'BC + A'BC'$ 2

(ii) $(A' + B)(A + B)$ 2

(iii) $X = B + A{\cdot}B' + A{\cdot}B$ 2

(iv) $(125)_R = (203)_S$, find out the value of radix R. 2

(d) The message below has been coded in the even parity humming code transmitted through a noise channel. Code the message assuming that it must have a single error occurred in each word code. (0111001) 8

Unit-II

2. (a) Distinguish between sum-of-products and product-of-sums. 4

(b) Implement the following function with a Multiplexer. 8

$$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$$

(c) Simplify the expression given below using K map. 8

$$Y = \sum m(0, 1, 5, 9, 13, 14, 15) + d(3, 4, 7, 10, 11)$$

(d) Determine the prime - implicates of the function. 8

$$F(W, X, Y, Z) = \sum(1, 4, 6, 7, 8, 9, 10, 11, 15)$$

Unit-III

3. (a) What is basic function flip-flop? 4

(b) Convert T FLIP-FLOP to D FLIP-FLOP. 8

(c) Explain JK flip-flop with suitable logic diagram, & explain its operation. 8

(d) Explain right counter & also explain synchronous counters. 8

Unit-IV

4. (a) Explain digital to analog converter. With suitable example. 4

(b) Explain weighted resistor/converter. 8

(c) Describe A/D converter with example. 8

(d) Explain R-2R Ladder D/A converter. 8

Unit-V

5. (a) Explain memory organization. 4

(b) What is programmable logic array? How it differs from ROM? 8

(c) Explain classification and characteristics of memories with example. 8

(d) Explain ROM & also explain types of ROM. 8

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B028312(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(Electronics & Telecommunication Engineering Branch)

ELECTRONICS DEVICES

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

***Note** : All questions are compulsory. Part (a) of each question is compulsory and attempt any two parts from parts (b), (c) and (d). Part (a) is of 4 marks and part (b), (c) and (d) each are of 8 marks. Assume suitable data whenever required.*

Unit-I

1. (a) A potential difference of 10 V is applied longitudinally to a rectangular speciman of intrinsic germanium of length 25 mm, width 4 mm and thickness 1.5 mm. Find the total current if intrinsic carrier concentration

is $2.5\times10^{19}/m^3$, $\mu_e = 0{\cdot}38\,m^2\ V^{-1}s^{-1}$, $\mu_h = 0{\cdot}18\ m^2V^{-1}s^{-1}$.

(b) Draw the energy band diagram of an open circuited p-n junction. Indicate Fermi level and contact potential E_0?

(c) In intrinsic GaAs, the electron and hole mobilities are 0.85 and 0.04 m^2/V-s respectively and corresponding effective masses are 0.068 m_0 and 0.5 m_0 respectively where m_0 is the rest mass of an electron. If the energy gap of GaAs at 300 K is 1.43 eV, calculate the intrinsic carries concentration and conductivity.

(d) Derive the following expression for a step graded junction $V_0 = V_T \log_e \left(\frac{N_A N_A}{n_i^2}\right)$.

Unit-II

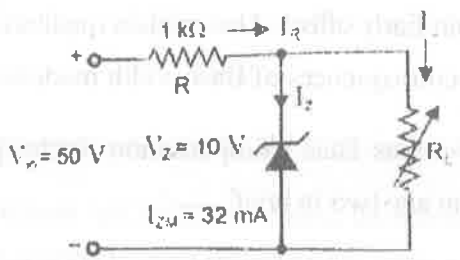
2. (a) (i) Define ripple factor and transformer utilization factor.

(ii) Why π -filters are not suitable for varying loads?

(b) Describe bridge rectifier. How does it differ from full wave rectifier using two diodes only? What do you understand by PIV?

(c) Explain the working of zener diode as a voltage regulator?

(d) For the network shown in below figure, determine the range of RL and IL that will result in VRL being maintained at 10 V, also determine the maximum wattage rating of diode.



Unit-III

3. (a) Explain following terms :

(i) Operating Point

(ii) Punch through

(iii) Thermal Runaway

(iv) Advantage of CE over CB and CC

(b) (i) Draw and explain the current components in a pnp transistor?

(ii) For a certain npn transistor $I_C = 5$ mA, $I_B = 50$ μA and $I_{CBO} = 1\mu A$.

Calculate α, β and I_E. Determine the new level of I_B required to make $I_C = 10$ mA.

(c) Explain Early effect. Also explain qualitatively the three consequences of Base width modulation?

(d) List various Bias Compensation Technique and explain any two in brief.

Unit-IV

4. (a) (i) Why FET is called a voltage controlled device?

(ii) Explain why does the drain current I_D not reduced to zero even after the channel is pinched off?

(b) Explain drain characteristics of n-channel JFET. Explain shape of characteristics and identify regions.

(c) (i) Compare JFET with BJT.

(ii) Why input impedance of FET is high?

(iii) Obtain the expression for the Pinch OFF voltage V_P in case of n-channel JFET?

(d) An n-channel JFET has $I_{DSS} = 10$ mA and pinch off voltage $V_P = -4$ V. Find the drain current for $V_{GS} = -2$ V. If transconductance g_m of a JFET with the same I_{DSS} at $V_{GS} = 0$ V is 4 m Mho, find the pinch off voltage.

Unit-V

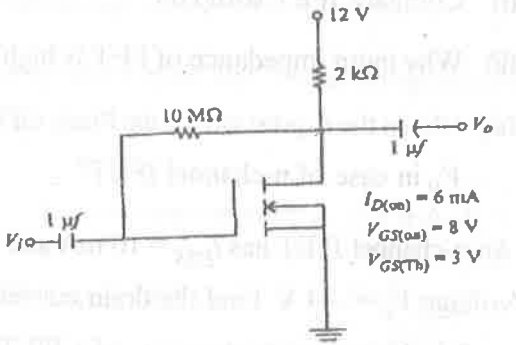
5. (a) Explain working of MOSFET as a switch.

(b) (i) Which MOSFET is called as Normally ON MOSFET and NORMALLY OFF MOSFET and why?

(ii) Make comparison between JFET and MOSFET.

(c) Define Pinch OFF voltage, threshold voltage and draw drain characteristics and tansfer characteristics for *n*-channel *E* MOSFET.

(d) Determine I_{DQ} and V_{DSQ} for Enhancement type MOSFET for given circuit.



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B028313(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(Electronics & Telecommunication Engg. Branch)

DIGITAL SYSTEM DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) of all the questions is compulsory. Part (a) carries 4 maks. Attempt any **two** from from part (b), (c) and (d). Part (b), (c) and (d) carries 8 marks each.*

Unit-I

1. (a) Perform the following BCD addition : 8 4

(i) 26 + 13

(ii) 579·6 + 636·8

(b) Prove the following Boolean expression : 8

(i) $A + A'B = A + B$

(ii) $AB + A'C + BC = AB + A'C$

(c) Reduce the expression

$$f = \sum m(1, 5, 6, 12, 13, 14) + d(2, 4)$$

and implement the real minimal expression using universal logic. 8

(d) Realize the XOR function using :

(i) AOI Logic,

(ii) NAND Logic, and

(iii) NOR Logic 8

Unit-II

2. (a) Design Full Adder using two Half Adders. 4

(b) Design a 4-line-to-16-line Decoder using 3-line-to-8-line Decoder. 8

(c) Implement the following logic function using an 8XI MUX

$$F(A, B, C, D) = AB' + BD + B'CD'$$ 8

(d) Design 4-bit BCD Adder and draw its logic diagram. 8

Unit-III

3. (a) What is meant by race around condition in flip flops and how this problem can be eliminated? 4

(b) Convert J-K flip flop to S-R Flip flow. 8

(c) Design a 4-bit universal shift register and draw the logic circuit diagram. 8

(d) Design a Synchronous BCD Counter using J-K Flip flops. 8

Unit-IV

4. (a) Define Mealy model and Moore model. 4

(b) What is a serial adder? Explain its working with the help of a state diagram and a state table. 8

(c) Draw and explain the ASM chart for sequence detector. 8

(d) Design 3-bit odd parity generator with the help of a state diagram and a state table. 8

Unit-V

5. (a) Compare the logic families in terms of commonly used specification parameters. 4

(b) With the help of a neat diagram, explain the working of IIL NAND and NOR Gates. 8

(c) With the help of a neat diagram, explain the working of a two-input TTL NAND gate with Totem-pole output. 8

(d) With the help of a neat diagram, explain the working of a two-input ECL OR/NOR gate. 8

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B028314(028)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2021

(AICTE Scheme)

(Electronics and Telecommunicaton Engg. Branch)

NETWORK THEORY

Time Allowed : Three hours

Maximum Marks : 100

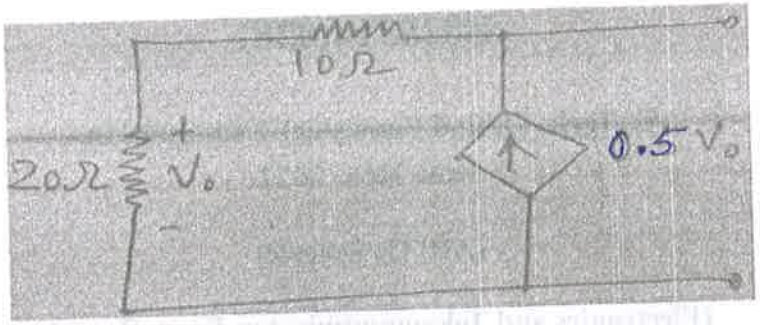
Minimum Pass Marks : 40

Note : *Attempt all questions. Part (a) of each question is compulsory and carries 4 marks. Solve any* ***two*** *parts from part (b), (c) & (d) and carries 8 marks each.*

Unit-I

1. (a) Write down the condition for maximum power transfer.

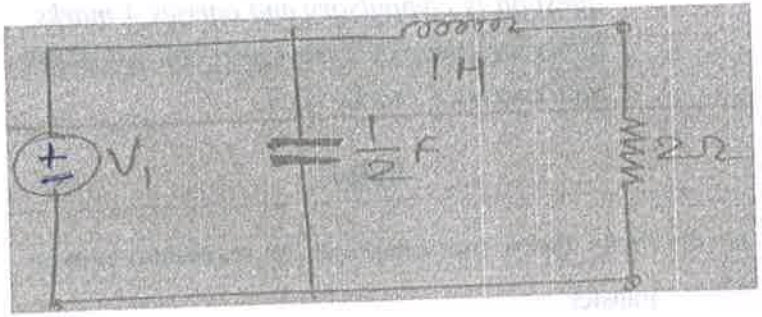
(b) Find out the Thevenin's equivalent circuit for the given network :



(c) The network shown in below figure is operated in the sinusoidal steady state, with the element values given and $V = 100 \cos 2t$. Determine :

(i) The complex power delivered by the source.

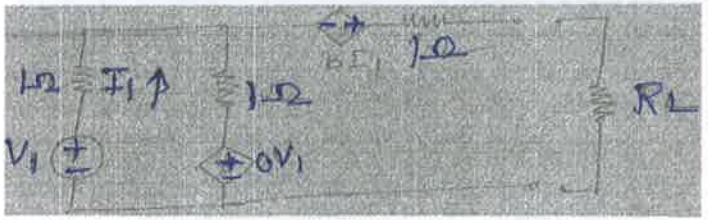
(ii) The effective current in each of the passive elements.



(d) For the given network shown that :

$$V_\theta = \frac{V_1}{2}[1 + a - ab] \text{ and } z_\theta = \frac{3-b}{2}$$

where V_θ = Thevenin's volt x, z_θ = Thevenin's resistance.

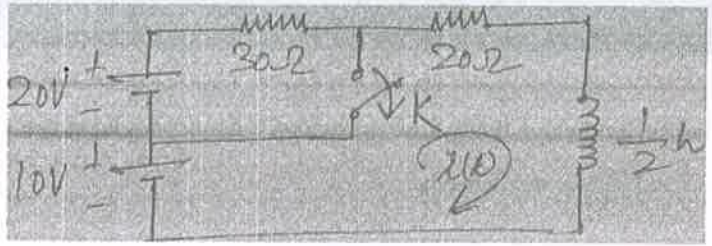


Unit-II

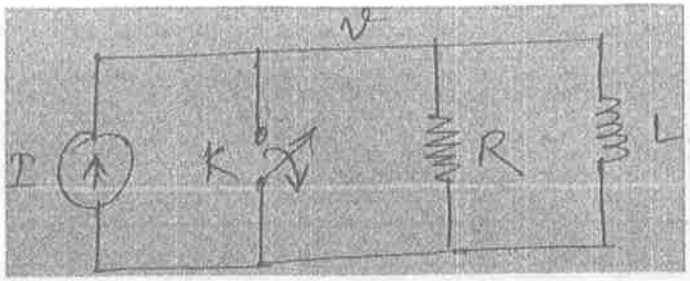
2. (a) What is the behaviour of inductor and capacitor under transient and steady state condition?

(b) Derive and explain the step response of RC circuit.

(c) The network of the figure reaches a steady state with the switch K open. At $t = 0$ the switch K is closed. Find $i(t)$ for numerical values given and sketch the current waveform. Also indicate the value of time constant.



(d) K is opened at $t = 0$, solve for V, dv/dt and d^2v/dt^2 at 0+, If $I = 1$ A, $R = 100\,\Omega$, $L = 1$H.

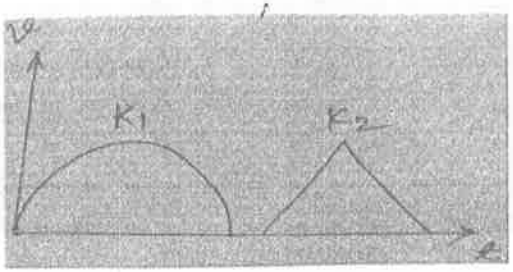


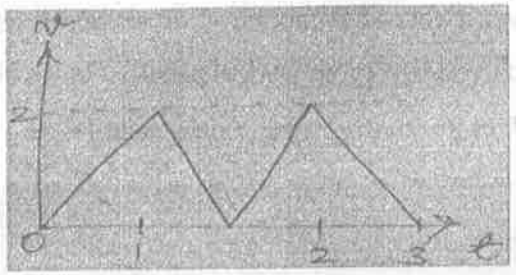
Unit-III

3. (a) Define initial and final value theorem.

(b) In the series RLC circuit shown, the applied voltage is $V(t) = \sin t$ for $t > 0$. For the elements values specified, find $i(t)$. The switch is closed at $t = 0$.

(c) Synthesize the following waveforms and find out the Laplace transform.



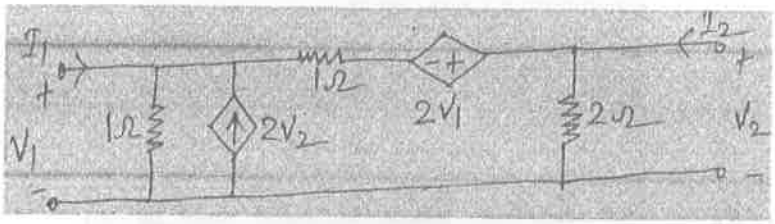


(d) State and prove Convolution Theorem. How does it useful for analysis of electrical network?

Unit-IV

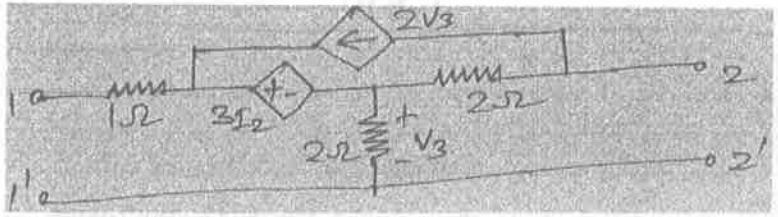
4. (a) Give the equations of h parameter.

(b) The figure shown contains both a dependent current and dependent voltage source. For the element values given, determine the Y and Z parameters :



(c) The network shown below consists of a resistive T and a resistive Π network in parallel. For the element values given, determine Y parameters :

(d) Determine Z and Y parameter for the given circuit :

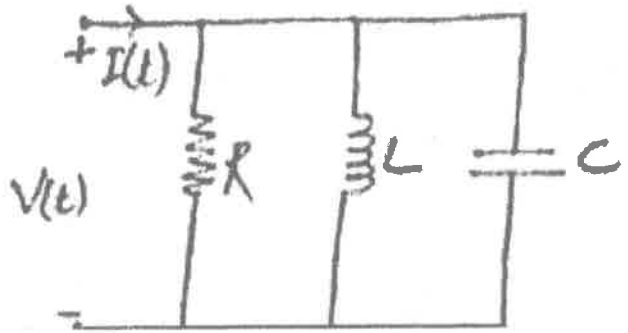


Unit-V

5. (a) What is a Sinusoid?

(b) Explain the basic principle behind sinusoidal steady state analysis. Also give the steps to be followed to find the steady state value of $i\ (t)$ in R-L circuit for a given excitation of $V = V \cos wt$, where V is the real time constant.

(c) For the given network find current.



Find : $I\ (t) = ?$

Given : $R = 1/3\ \Omega$

$L = 1/4$ H

$C = 3$ F

$V\ (t) = \sin 2\ t$

(d) Draw the phasor diagram of RL, RC and RLC circuit.

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B028315(028)

B. Tech. (Third Semester) Examination, Dec.-Nov. 2021

(AICTE Scheme)

(Electronics and Telecommunication Engg. Branch)

DATA STRUCTURES USING C++

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Attempt all questions. Every question has four parts. Part (a) is compulsory. Attempt any two parts from (b), (c) and (d).*

Unit-I

1. (a) Write the benefits of Object Oriented Programming. 4

(b) Define class and object. Explain the use of access specifiers (Public, private and protected with help of example. 8

(c) What do you mean by friend function? How it is declared, defined and called? Explain with example. 8

(d) What is Constructor? Explain types of constructor with example. 8

Unit-II

2. (a) Define Virtual base class. 4

(b) Write a C++ program to overload the '+' operator to add two strings. 8

(c) Explain function overloading with the help of an example. 8

(d) Define Inheritance. Explain the differences between Multiple and Multilevel Inheritance. 8

Unit-III

3. (a) Define abstract class. 4

(b) Develop a C++ Program to demonstrate the usage of *new* and *delete* operators. 8

(c) Explain Virtual functions with example. 8

(d) Write a C++ program demonstrating use of the pure virtual function with the use of base and derived classes. 8

Unit-IV

4. (a) Define Linear Search. 4

(b) Explain Binary search with the help of a C++ program. Give one example. 8

(c) Write a program to sort an array of integers using Bubble Sort. Also show the output for following array : 45, 10, 70, 5, 18, 75, 55, 4, 60, 2 8

(d) Explain how to implement Circular queue and Priority Queue with suitable example. 8

Unit-V

5. (a) Define Linked Lists. 4

(b) Describe the implementation of a binary search tree with the help of an example. 8

(c) Explain sequential representation of graph using 8

(i) Adjacency matrix

(ii) Adjacency list

(d) Explain BFS and DFS graph traversal techniques with the help of example. 8